FIG.1

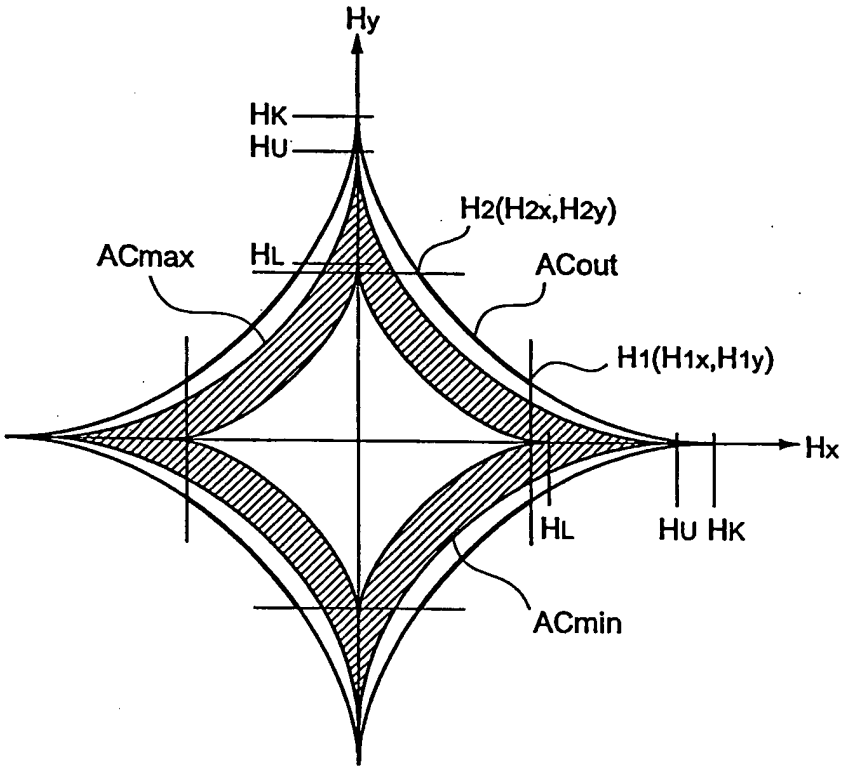


FIG.2

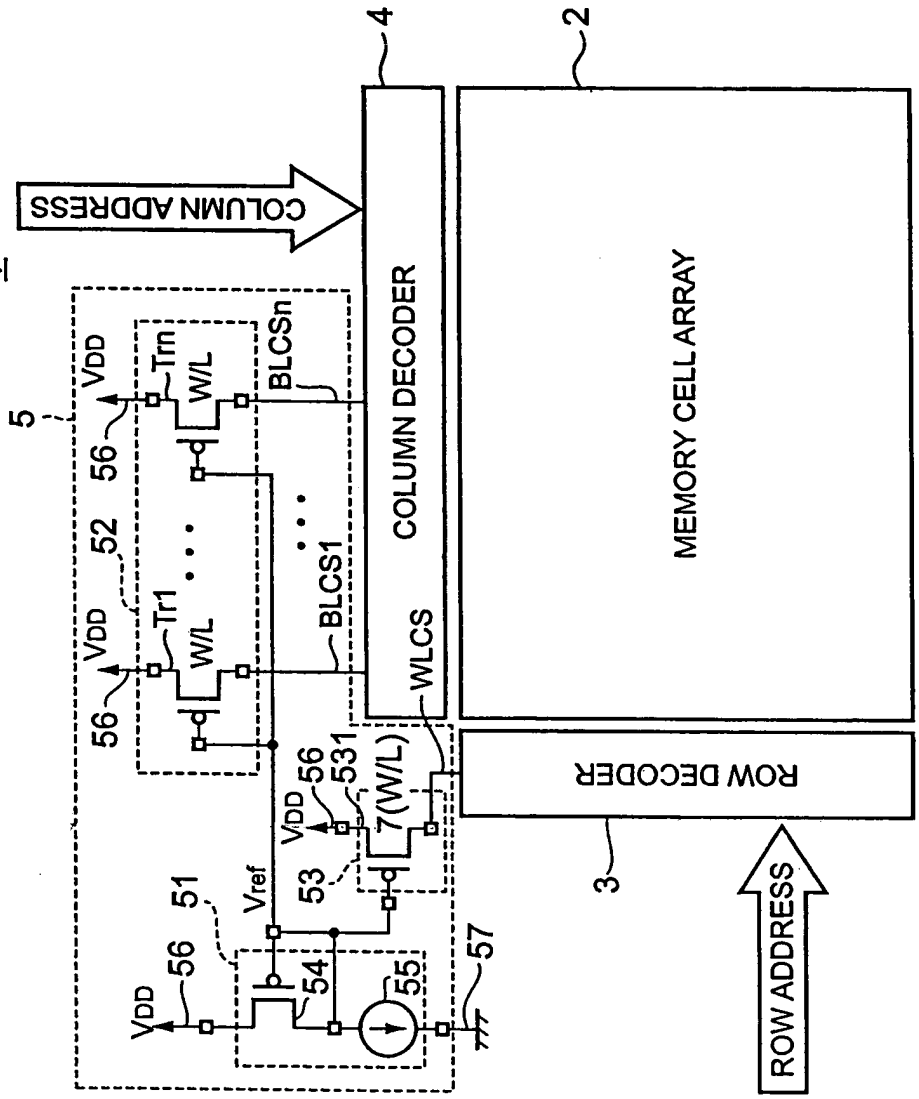

1
2
3
4
5
COLUMN ADDRESS
COLUMN DECODER
MEMORY CELL ARRAY
ROW DECODER
ROW ADDRESS
WLCS
BLCS1
BLCSn
Tr1
Trn
W/L
VDD
Vref
51
52
53
54
55
56
57
531
7(W/L)

FIG.3

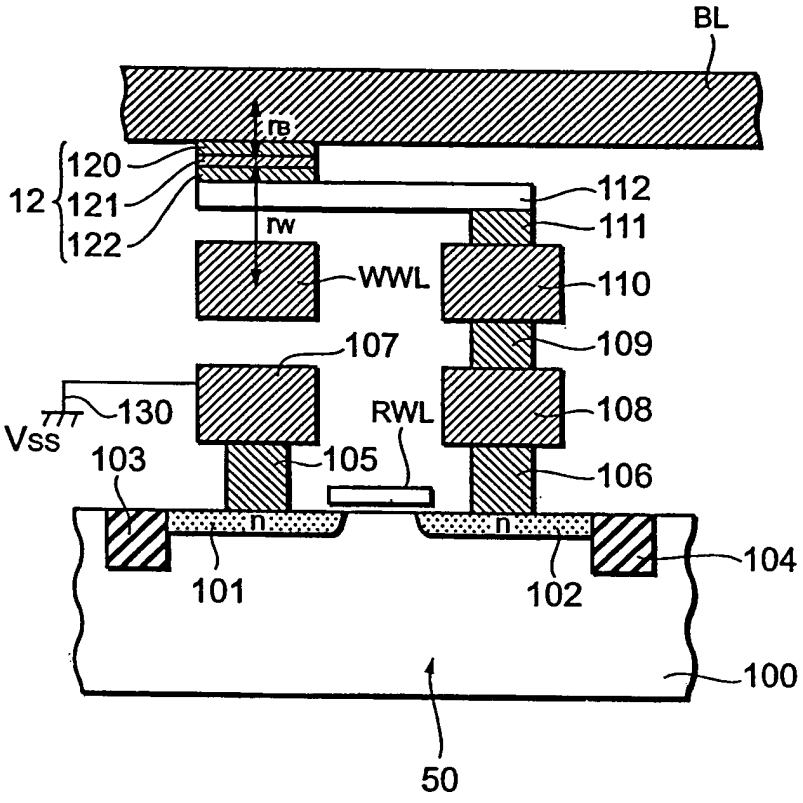

BL
rB
120
121
122
12
112
111
rw
WWL
110
109
107
130
Vss
RWL
108
103
105
106
n
n
104
101
102
100
50

FIG.4

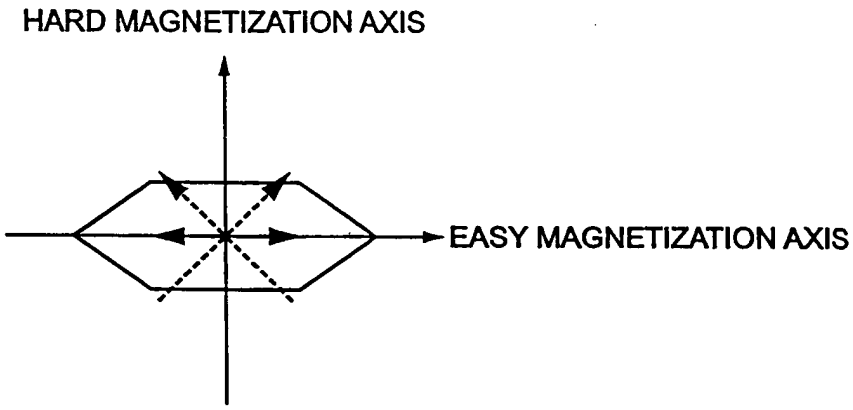

HARD MAGNETIZATION AXIS
EASY MAGNETIZATION AXIS

FIG.5

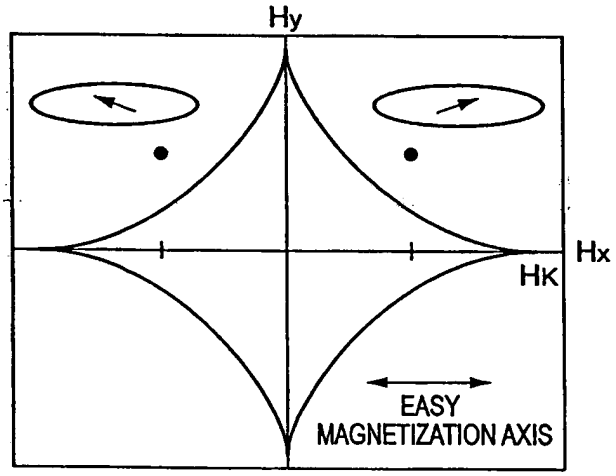

Hy
Hx
HK
EASY
MAGNETIZATION AXIS

FIG.6

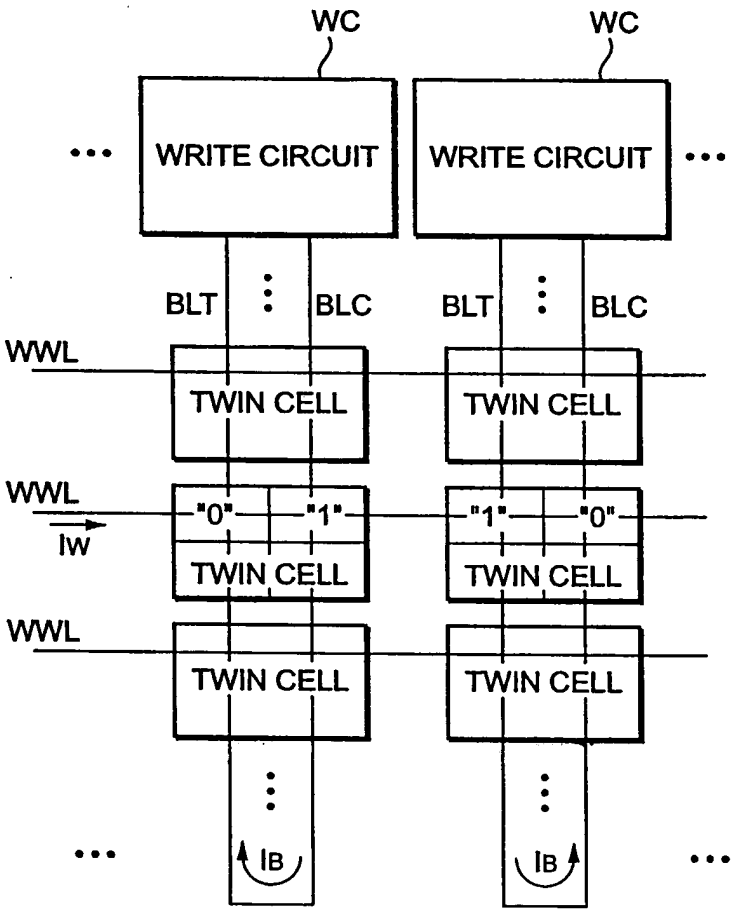
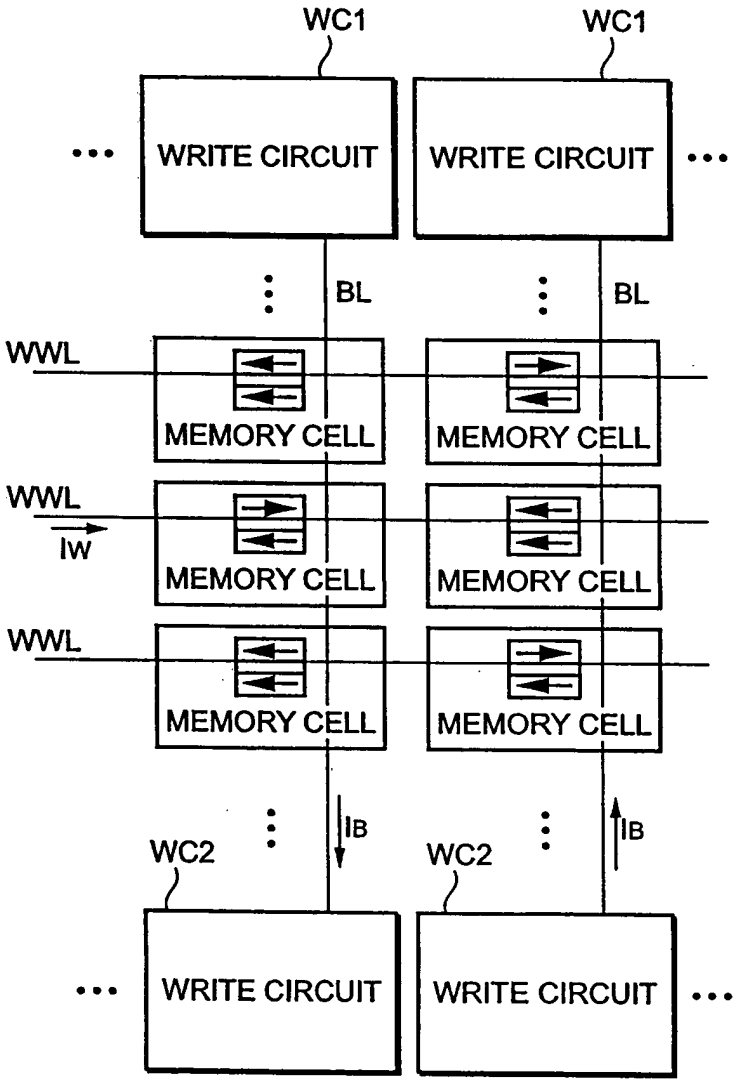

WC
WC
WRITE CIRCUIT
WRITE CIRCUIT
BLT
BLC
BLT
BLC
WWL
TWIN CELL
TWIN CELL
WWL
"0"
"1"
"1"
"0"
IW
TWIN CELL
TWIN CELL
WWL
TWIN CELL
TWIN CELL
IB
IB

FIG.7


WC1
WC1
WRITE CIRCUIT
WRITE CIRCUIT
BL
BL
WWL
MEMORY CELL
MEMORY CELL
WWL
Iw
MEMORY CELL
MEMORY CELL
WWL
MEMORY CELL
MEMORY CELL
IB
IB
WC2
WC2
WRITE CIRCUIT
WRITE CIRCUIT